

DoD's Challenges and Approach to Expanding the National Microelectronics Ecosystem

Shaping the Future of Manufacturing Using High Performance Computing Workshop

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CRITICAL TECHNOLOGY SYNERGIES: MICROELECTRONICS







T&AM Program Enabling Access to State of the Art (SOTA)





Access to State of the Art (SOTA) Roadmap: Microelectronics

Fiscal Years -> 2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032+
Foundry Access	Access to SOTA US commercial foundries for DoD specific designs (Intel & Global Foundries)									
	Fund 2-3 runs node technolo	Establish 2 runs per year in commercial ≤5nm node technology for DoD Specific Designs								
RAMP	Rapid Assured Microelectronics Prototypes (Microsoft Team, Qualcomm)									
	Demonstration of sec prototypes by the DIB	ure design ca in SOTA teo	apability via hnology	3	Cloud bas design an	sed commen nd manufactu	cially scalabl uring flow cap	e, quantifial Dability fully	bly assured, utilized by Di	В
RAMP-C	RAMP-Commercial (Qualcomm, Intel)									
Indications of Technology Lasterite Indications	Intel 18A test chip designs completed	tel 18A PDK	18A PDK	High Volun foundry caj DoD ICs	ne (25k/wpm pability for Q.	s) leading eo A dual-use (dge (<5nm) COTS & custom			
Emulation and EDA	Emulation Pathfinder for QA Design Flow (AFRL)									
	JSF F35 & PEO SUB based QA design flow	prototype de 's	monstration	s of emulatio	n Qua desi	lified emulat gn flow capa	ion based QA bility	4		
SAHARA	Structured Array Hardware for Automatically Realized Applications (Intel)									
	Prototype Structured demonstrated (50M g	Array chip ates)		A Fi de	ully develope esigns to Stru	d SAHARA (uctured ASIC	capability to e C, at an onshe	efficiently co ore SOTA fo	onvert existing oundry with se	g FPGA ecurity
Design Acceleration and Transition	New Starts in FY23 – Design Acceleration and Transition Efforts Contract awards(s) for new T&AM activities									
LEGEND	LEGEND Major Investments to Mature the Domestic SOTA Future SOTA Microelectronics Ne									Needs
Enhanced Capabilities	Microelectronics Ecosystem Ecosystem alignment to DIB and POR							naterials, DR		

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NorthPole Neuromorphic Architecture Advantages

Conventional Von Neumann Processors

- Not capable of achieving the required SWAP parameters due to physically separate memory and computation components
- Processing efficiency limited by data exchange bottlenecks

NorthPole: a Non-Von Neumann Processor

- Incorporates neuromorphic, brain-inspired revolutionary architecture with co-located computation and memory devices
- Dramatically increases SWAP efficiency

DoD Systems Increasingly Require High-Performance Edge Processing for More Capable Operational Applications

- Adversaries are fully embracing this military enhancing leap ahead technology – one that we cannot afford to let go unanswered
- Commercial microelectronics components are too SWAP-limited to satisfy this need



NorthPole Architecture Performance Dominates Competitors

- Conventional Processors provide incremental performance gains through costly microelectronics technology scaling
- NorthPole Vastly Outperforms Conventional (V100) Processor
 - 5x greater computational performance
 - 23x greater energy efficiency





Access to Advanced Packaging Roadmap: Microelectronics





Heterogeneous Integration (HI) and SWAP Benefits

Why HI?

- Modular approach vs. Monolithic approach
- Not every logic function (IP) needs to be designed in the same process node (HI)
- Leveraging IP in the form of chiplets
- Current industry trend has led to chiplets on silicon interposers
- Includes latest IC packaging 2.5D, 3D, FOWLP technologies
- Optimize nodes required for ideal performance and cost



Notional HI MCP

SHIP is leveraging commercial HI solutions to improve SWAP savings and system performance



Expected SWAP Savings: 8x relative to current solution

Through HI enabled SWAP savings, MCP-1 will deliver:

- Unprecedented spectral agility
- ✓ Enhanced signal processing
- ✓ Lower power consumption
- Improved thermal management

SHIP-D functional parts have been delivered to lead DIB partner to prove SWAP benefits



MCP-1 consisting of two chiplets integrated with an FPGA

MCP-1 finished package

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CHIPS Offers a Whole of Government Approach

THE OFFICE OF THE DEPUTY TECHNOLOGY OFFICER FOR CRITICAL TECHNOLOGIES

The NSTC and Microelectronics Commons will expand the number of concepts and ideas that can transition from proof-of-concept to the market.





Microelectronics Commons Addresses the Valley of Death

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Required Investment

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"Valley of Death"

Prototype in a

Foundry/Fab

Prototype in

Laboratory



Microelectronics Commons Accomplishments

https://microelectronicscommons.org





Establishment of Microelectronics Commons Program

(U) Microelectronics Commons Request for Solution (RFS)

- The Microelectronics Commons RFS was released on November 30, 2022. Solutions were received and the RFS was closed on February 28, 2023
- Source Selection Determination Completed

(U) Industry Days and Upcoming Commons Meeting

- Industry Days were successfully conducted on December 7 - 8, 2022. The event saw both senior leadership and significant interagency participation. There were **more than 900 participants in attendance** at this hybrid event held at the Ronald Reagan Building and International Trade Center in Washington, D.C.
- The Inaugural Microelectronics Commons Meeting is being held on 17-18 October 2023 in Washington, DC

The Microelectronics Commons is Now a Reality

(U) The Deputy Secretary of Defense announced 8 Hub Award Winners on 20 September 2023

- Arizona State University led Southwest Advanced Prototyping or SWAP Hub – \$39.8 million
- Midwest Microelectronics Consortium (MMEC) Hub \$24.3 million
- North Carolina State University led Commercial Leap Ahead for Wide Bandgap Semiconductors (CLAWS) Hub – \$39.4 million
- The Applied Research Institute led Silicon Crossroads Microelectronics Commons Hub – \$32.9 million
- Stanford University led California-Pacific-Northwest AI Hardware or Northwest AI Hub – \$15.3 million
- The Massachusetts Technology Collaborative led Northeast Microelectronics Coalition Hub – \$19.7 million
- The State University of New York led Northeast Regional Defense Technology or NORDTECH Hub – \$40 million
- The University of Southern California led California Defense Ready Electronics and Microdevices Superhub (DREAMS) Hub – \$26.9 million



Progression from Concept to Capabilities

OUSD (R&E)'S MICROELECTRONICS PROGRAMS ARE ALIGNED TO DEVELOP AND DELIVER NEW DEFENSE CAPABILITIES.



Lab-to-fab prototyping bridges valley of death from laboratory research to foundry/fab prototyping

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