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Opportunities for HPC in the design and manufacturing of semiconductor systems

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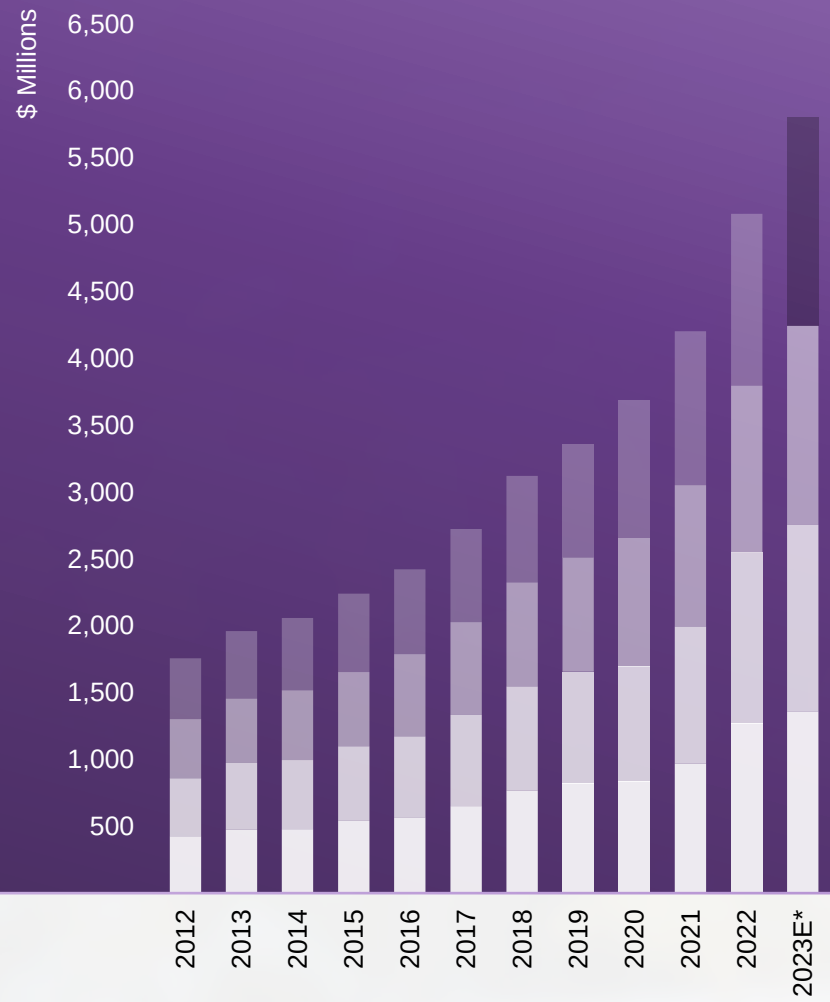
Synopsys overview



$5.8B
Revenue (TTM)

19,985+
Employees

3,322
Patents

118
Offices

#1 Electronic design automation tools and services

Broadest IP portfolio and #1 interface, foundation and physical IP

Leader in Gartner's Magic Quadrant for application security testing

Towards “Lights Out” Fabs

COLLECT

- Data Collection & Planning
- Data Contextualization
- Data Integration

Data Management

CONTROL

- Trace Process Control
- Statistical Process Control
- OCAP Control
- Dynamic Fault Detection
- Run to Run Process Control
- Recipe Management

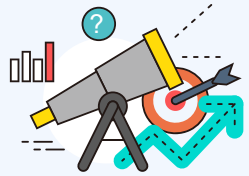
Process Control

ANALYZE

- Defect Data Management
- Yield Analysis
- Root Cause Analysis:
  Data Mining,
  Trace Analysis
  Chamber Matching Analysis

Yield & Root Cause Analytics

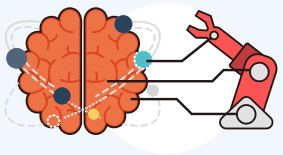
PREDICT



- Predictive Maintenance
- Yield Prediction
- Decision Support
- Virtual Metrology

Predictive Process Control

AUTOMATE



- Engineering Automation
- Intelligent Decision Support
- Integrated Automation
  (IT+OT)

Adaptive Intelligence

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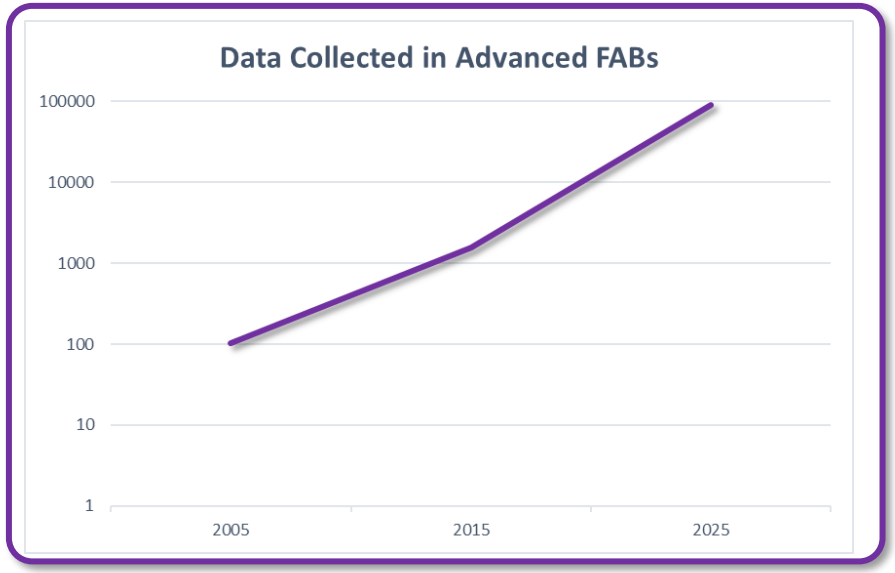
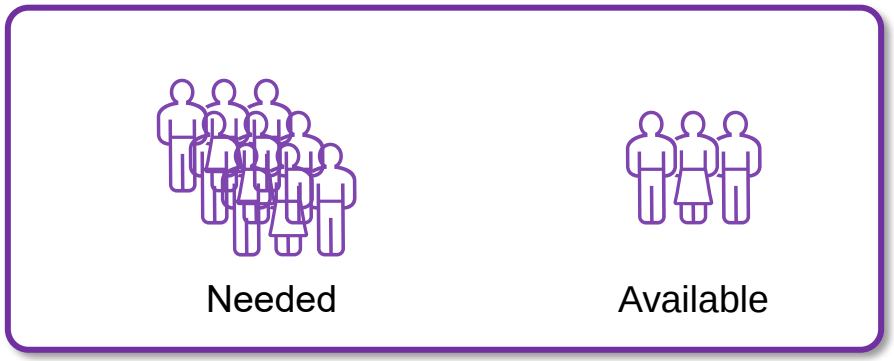
Conventional Process Control Solutions Struggling to Meet Industry Needs

Explosion of data collected in the fabs



Shortage of experts to run the fabs



- Solutions are not scaling with the needs of giga fabs
- Petabytes of data, thousands of manufacturing “tools”
- Analysis time for root cause takes longer
- Late or inaccurate decisions increase scrap and production cost
- Industry needs a new paradigm for process control

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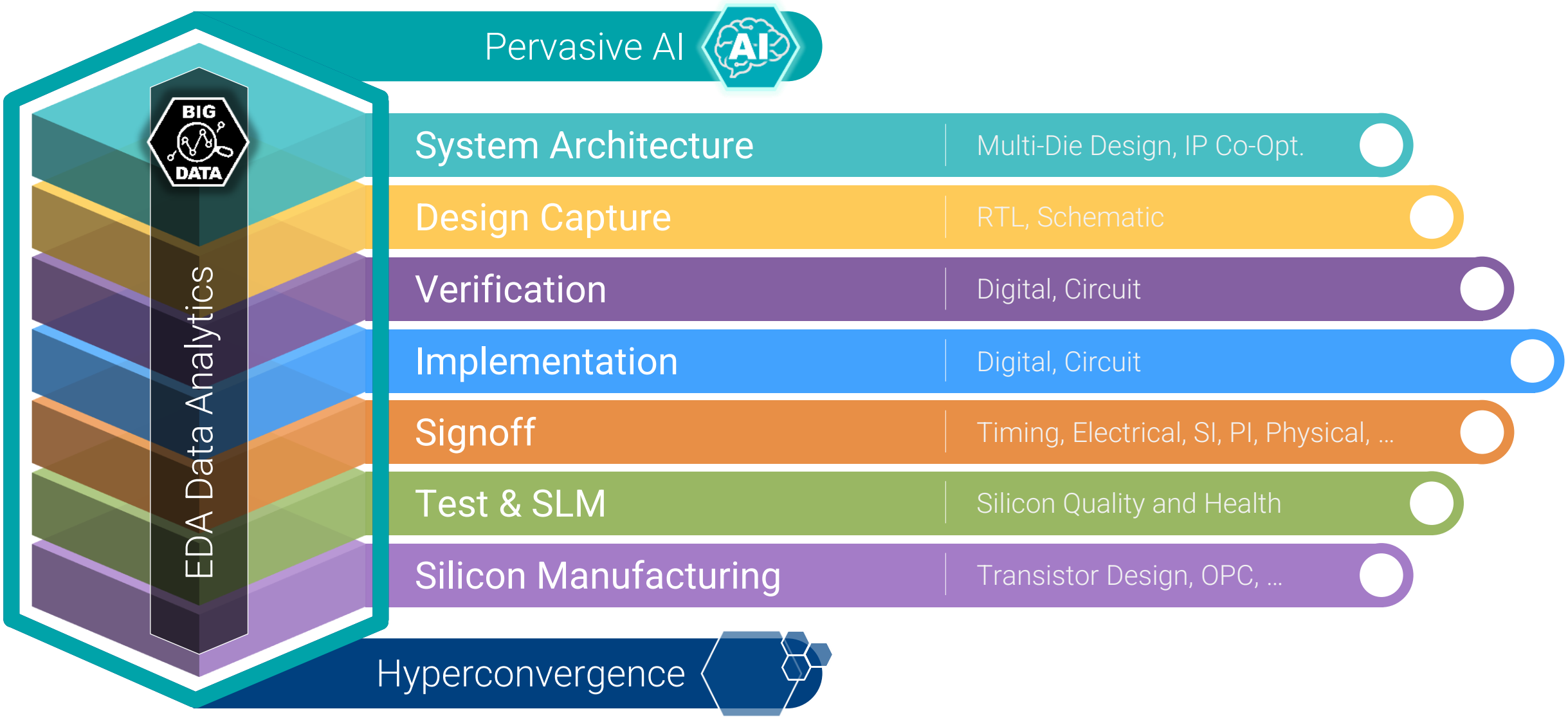
Electronic design automation flow



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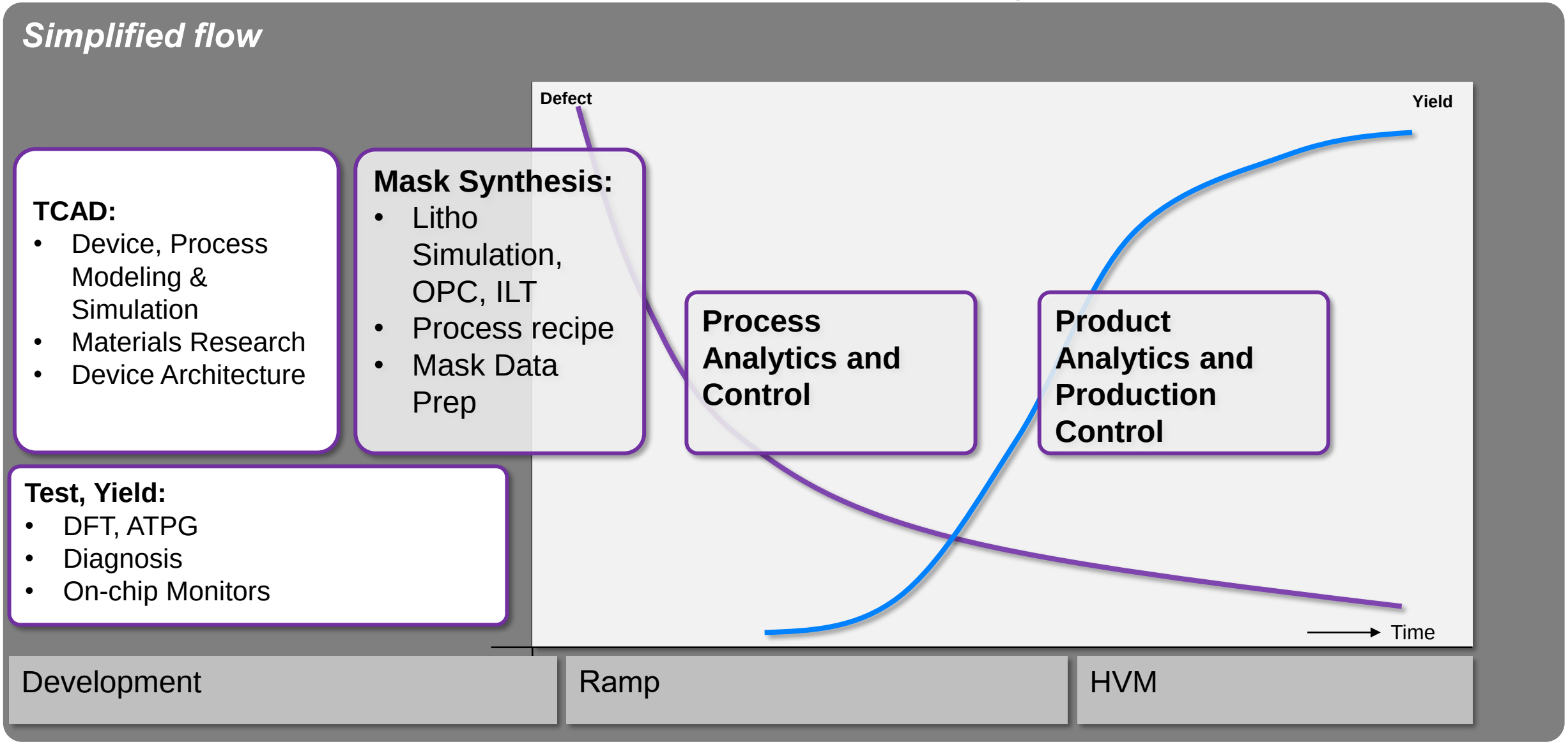
Software-centric view of IC Manufacturing

Simplified flow



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EDA algorithms at a glance

- Graph traversal, matrix solvers, compilers, database manipulation, …
- NP Hard, 40+ years of heuristics
  - Most originally developed with a single workstation, NFS worldview
  - Genetic algorithms, neural networks, deep learning etc. added/tried since the 1990s
- Massive scale
  - Millions to billions of instances, limited by compute capacity not problem size
  - Partitioning designs is a major implementation challenge
- Wide range of inherent parallelization possibilities
  - From straightforward to “nobody knows how”

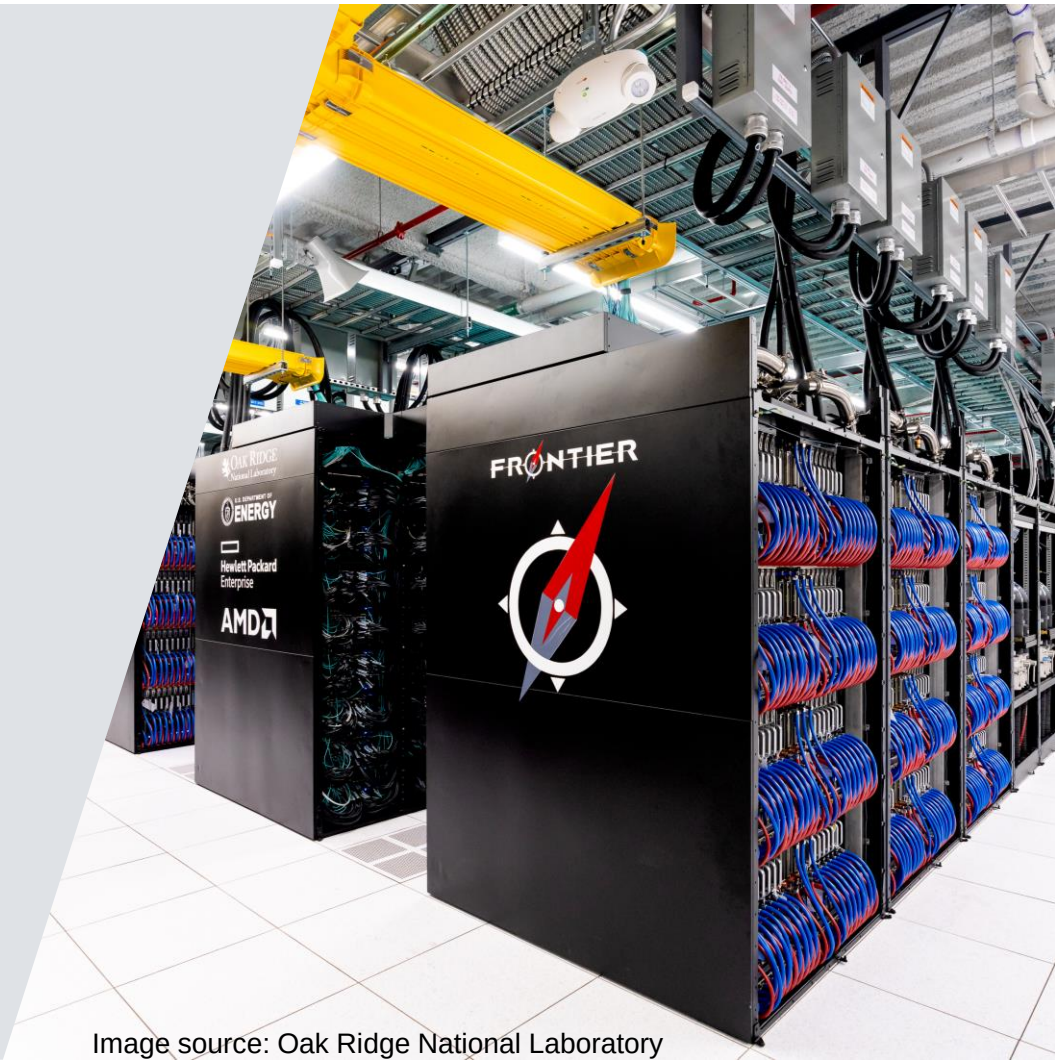

Image source: Oak Ridge National Laboratory

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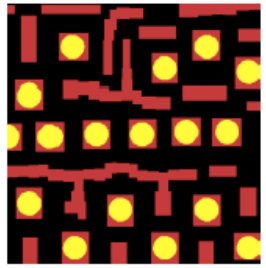
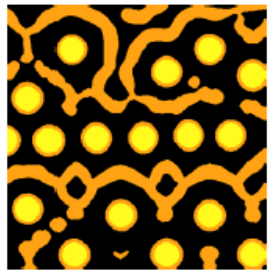
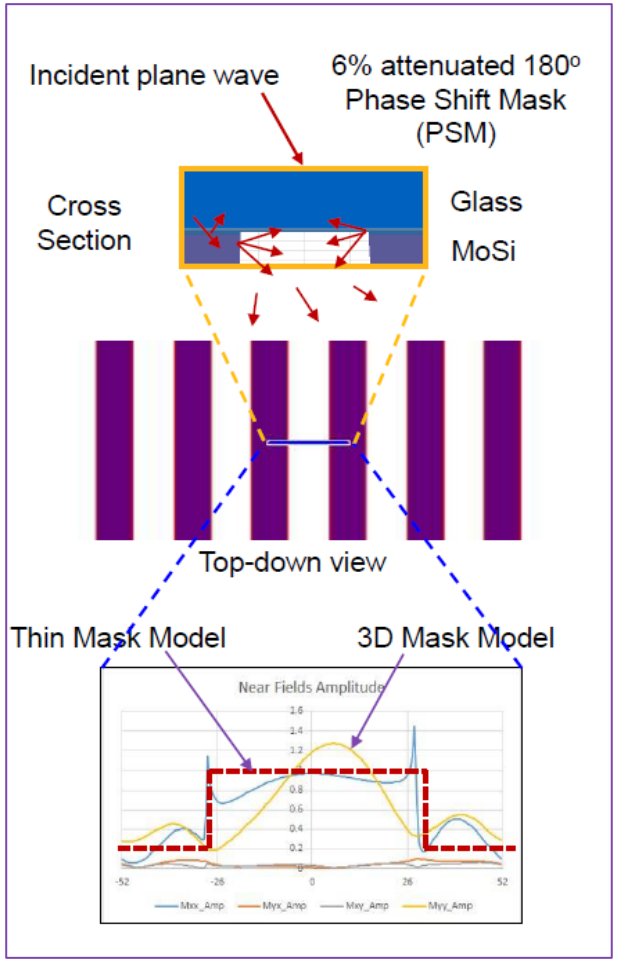
Example: mask making for lithography

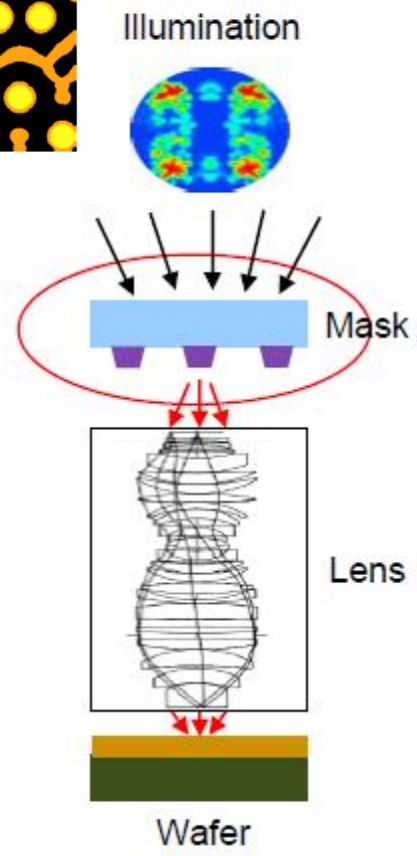
When what you see isn't what you get

- Hundreds of billions of features on a modern chip
- Optical lithography uses 193nm light to print much smaller features
- Designing masks (Inverse Lithography Technology, ILT) requires complex 3D manipulation of light, in theory solving Maxwell's equations
- Highly parallelizable
- Originally CPU based
- Algorithms can be restructured to be more GPU friendly
- Further optimization possible for customized accelerators









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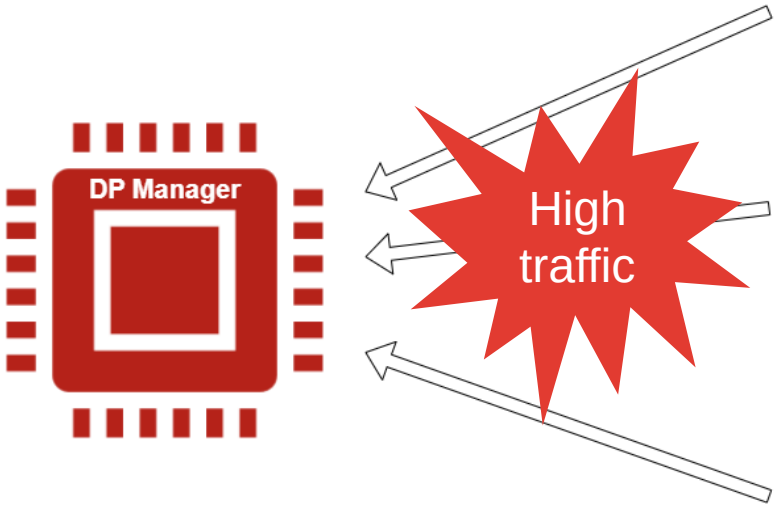
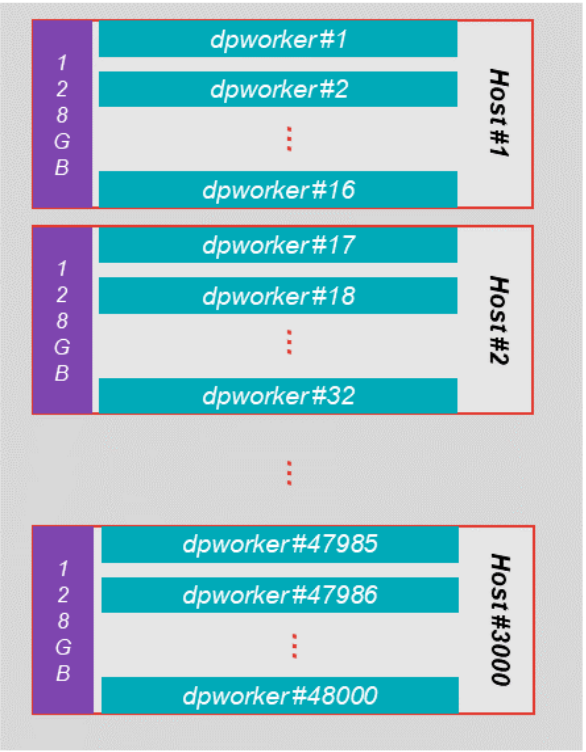
Expanding to datacenter scale

- Full chip (100B+ features) ILT can easily use 100k workers
- 24-hour turnaround desired
- After algorithm parallelization complete, Posix file system and communication to manager task biggest bottlenecks to scaling
- Intercept file system API to reduce communication and enable scaling to multiple datacenters





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Summary and future opportunities

- 40+ years of optimization in Electronic Design Automation
- Moore’s law kept a balance between problem complexity and solution capability
- Data and complexity explosion in semiconductor manufacturing
- Datacenter scale and AI/ML offer promise for HPC solutions

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