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U.S. DEPARTMENT OF ENERGY
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Optimizing Plasma-Assisted Semiconductor Chip Manufacturing

Revathi Jambunathan (PI)[1], Andrew Nonaka[1], Remi Lehe[1], Richard Lombardini[2], Andrea Diaz[2], Andrew Fierro[3], Jorge Quiroga[3], Tristan Jiron[3] and Mark Kushner[4]

1 Lawrence Berkeley National Laboratory, Berkeley, CA
2 St. Mary's University, San Antonio, TX
3 NMT University, Socorro, NM
4 University of Michigan, Ann Arbor, MI

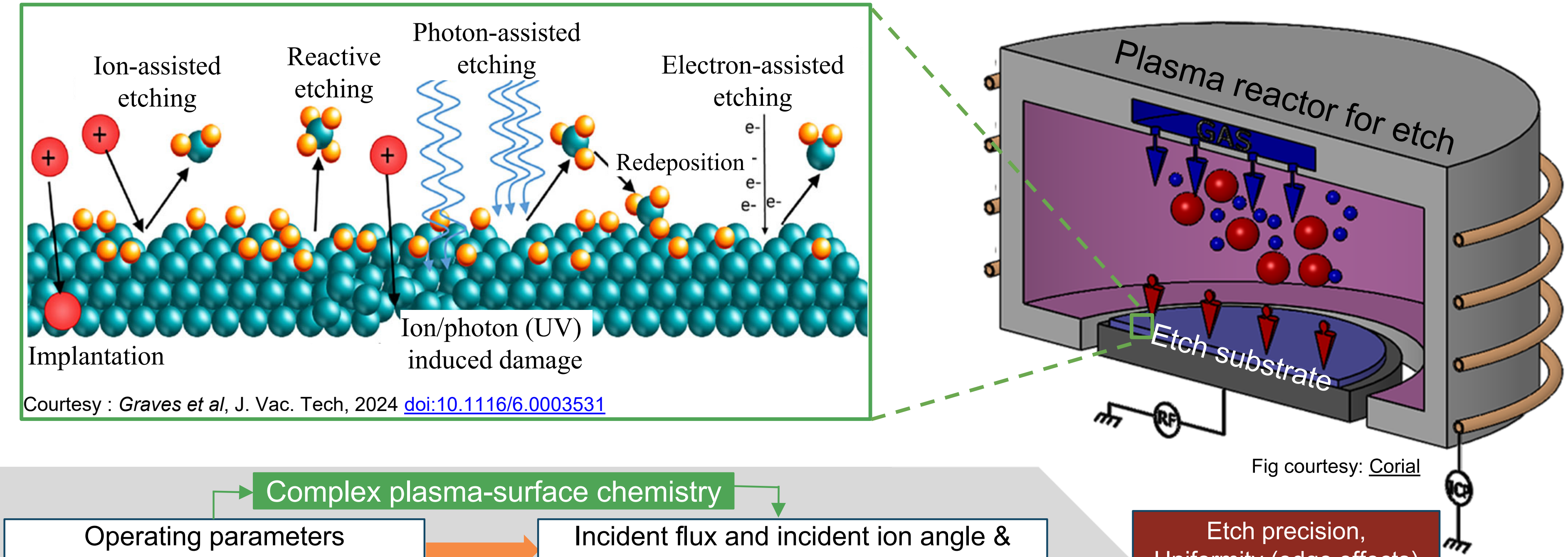
HPC4EI Workshop
25th February, 2026

HPC4 ENERGY INNOVATION

AMCR
Applied Mathematics & Computational Research

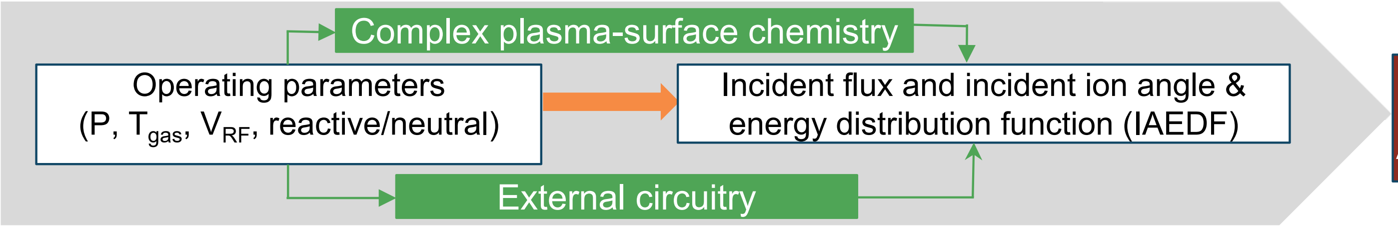
Need “digital twin” for optimizing complex chip fabrication

Current chip fabrication process design involves trial & error approach - costly and time consuming



Courtesy : *Graves et al*, J. Vac. Tech, 2024 doi:10.1116/6.0003531

Fig courtesy: Corial



Complex plasma-surface chemistry

Operating parameters (P, T_{gas}, V_{RF}, reactive/neutral)

Incident flux and incident ion angle & energy distribution function (IAEDF)

External circuitry

Etch precision,
Uniformity (edge effects)
Affects yield - cost & energy

Need for a virtual fabrication tool - “digital twin”:

(a) process design and optimization for high precision, high-yield

(b) investigations of complex near-surface physics

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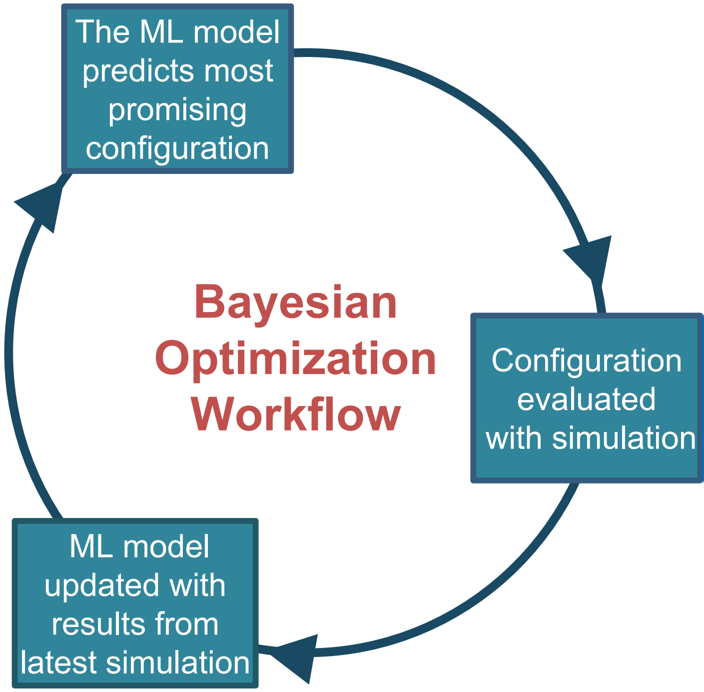
Digital twin framework : optimization + HPC

Fluid-based approaches cannot capture IAEDF
First-principles Particle-in-cell required



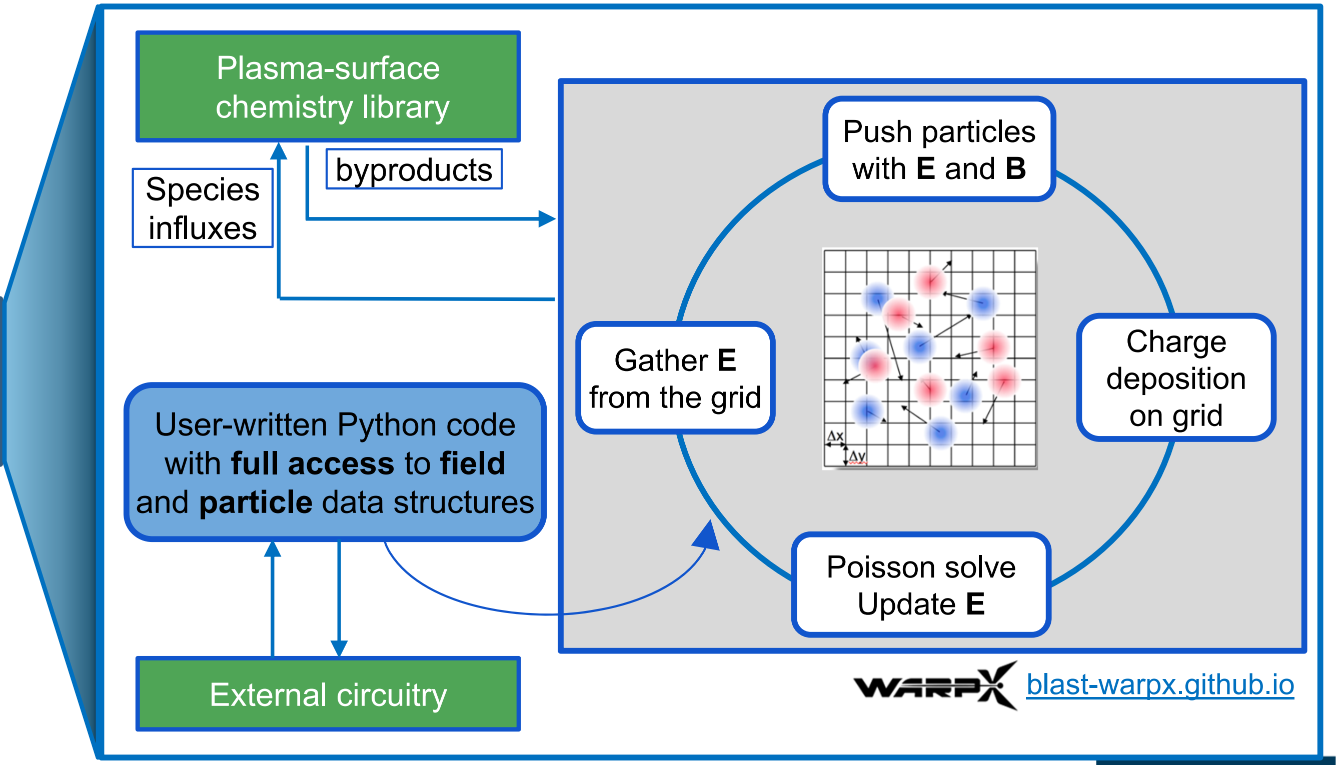
The ML model predicts most promising configuration

Configuration evaluated with simulation

ML model updated with results from latest simulation

Bayesian Optimization Workflow

github.com/optimas-org/optimas



Plasma-surface chemistry library

Species influxes

byproducts

User-written Python code with **full access** to **field** and **particle** data structures

External circuitry

Push particles with **E** and **B**

Charge deposition on grid

Poisson solve Update **E**

Gather **E** from the grid

WARPX blast-warpx.github.io

Opensource + industry compatible
BSD-3-Clause-LBNL licensing

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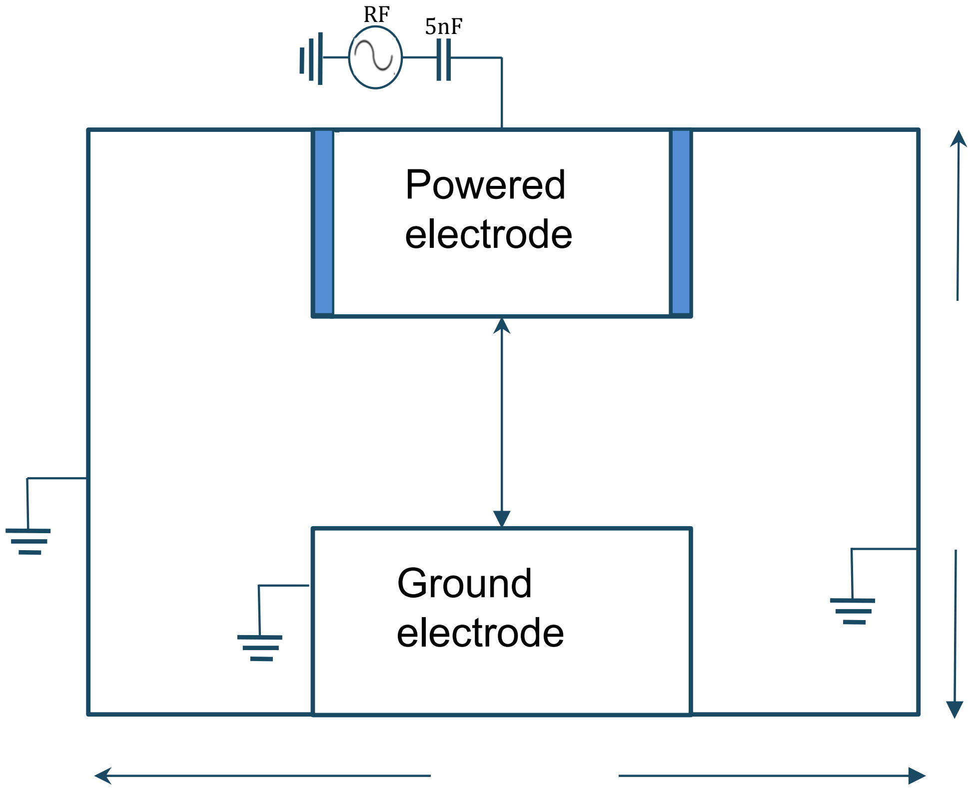
Plasma reactor set-up for kinetic simulations



Experimental operating parameters**

Powered RF Voltage : 100V; f = 13.56 Hz

Background pressure : 100mTorr

Kinetic simulation parameters

Grid : 256 X 128

Simulation time : 5000 RF cycles

Timestep (dt) : (1/400 f)

Initialized with ~1 Million particles

At the end 7.4 M particles

Monte Carlo Collisions for Argon chemistry

electrons : elastic, excitation, ionization

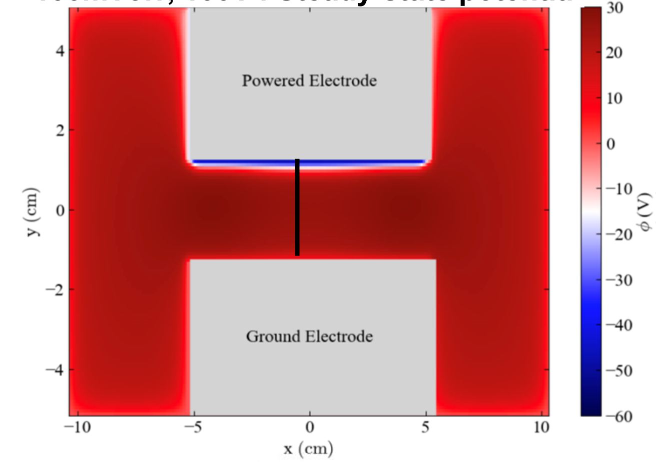
Ions: elastic, back-scattering

*Shahid Rauf, On uniformity and non-local transport in low-pressure CCP, PSST, 2020

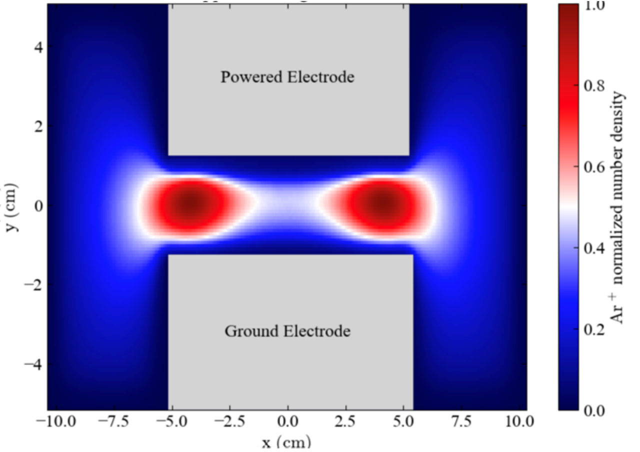
**P.J. Hargis et al., The GEC RF reference cell: A defined parallel plate RF system for expt and theoretical studies of plasma discharge, Rev of Sc.Instr, 1994

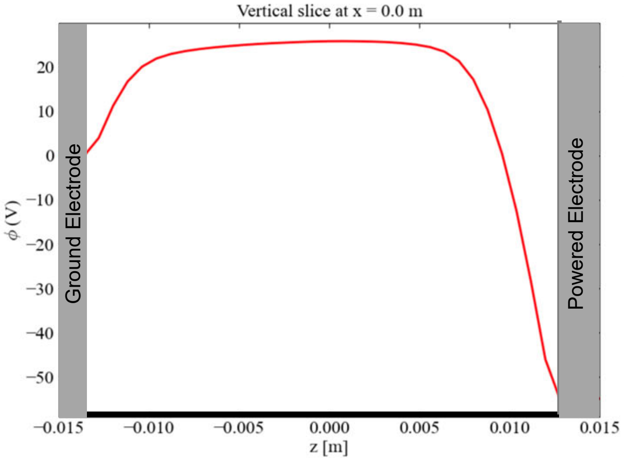
Capturing kinetic effects at reactor scale (100mTorr, 100V)

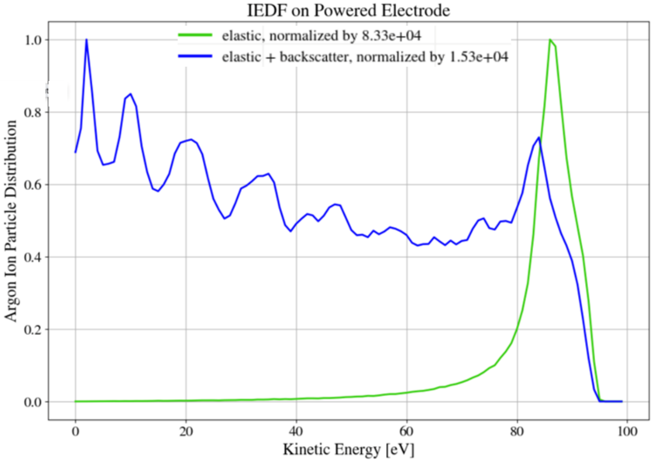
100mTorr, 100V : Steady-state potential



100mTorr, 100V : Steady-state normalized Ar⁺ density





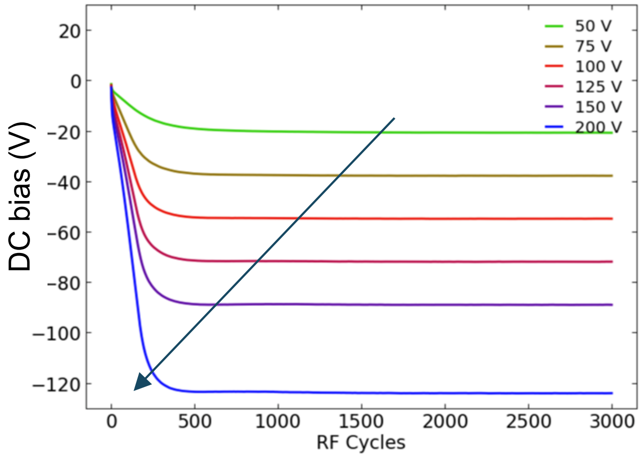


Simulations capture kinetic effects

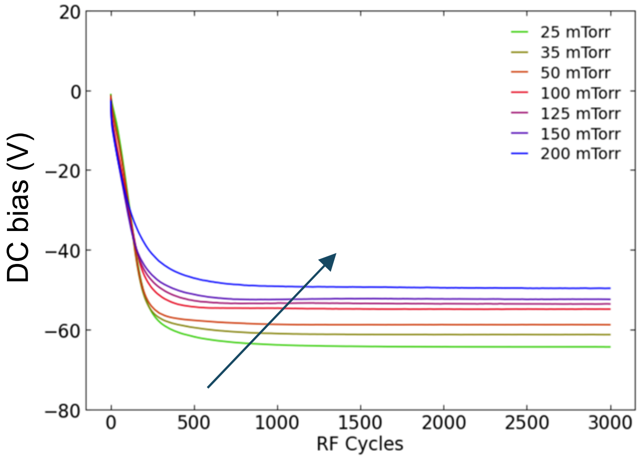
- DC bias voltage builds at powered electrode due to external circuit with capacitor
- Steady-state within 1000 RF cycles (73μs)
- IEDF peak ~ voltage drop at powered electrode for case with elastic collisions only
- Back-scattering damps high-energy and leads to resonant peaks
- Simulations were performed for 3000 RF cycles (0.2 ms) and required 17 hours of walltime

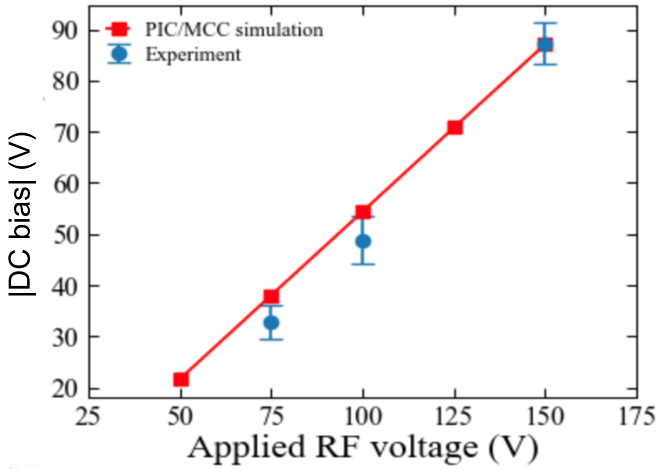
Simulated results agree with experiments

Voltage Scan, Pressure=100mTorr



Pressure Scan, Voltage=100V



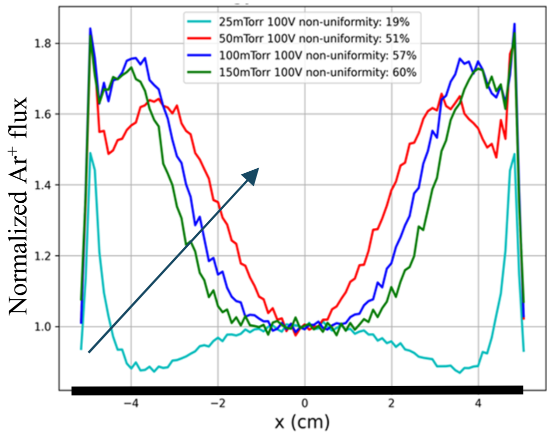


- Increase in V – *increases* DC bias
- Increase in P – *decreases* DC bias
- Simulated DC bias agrees with experimental measurements*

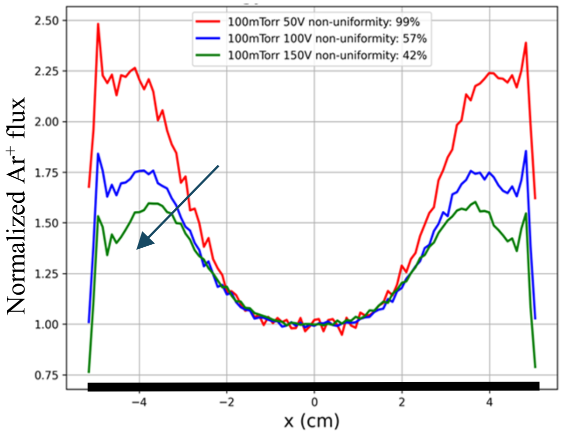
**Hargis P J et al 1994 Rev. Sci. Instrum*)

Identifying optimum parameters for etch uniformity

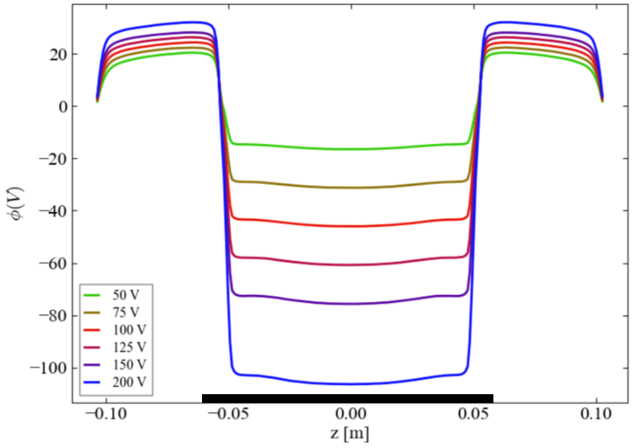
Higher P : *increases* Ar^+ flux non-uniformity

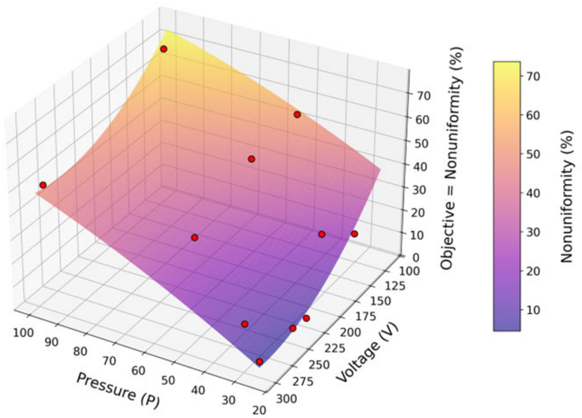


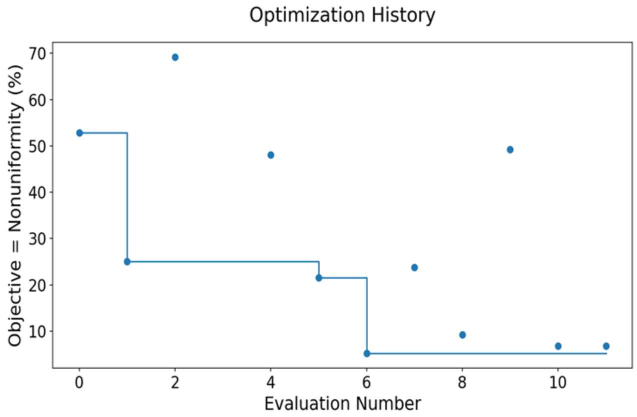
Higher V : *decreases* Ar^+ flux non-uniformity



Electric potential along powered electrode







ML-enhanced Bayesian optimization (BO) studies

Parameter space : P (25-200 mTorr) ; V (50-300 V)

Optimum value is 25mTorr, 300V

12 evaluations using GPU-accelerated HPC simulations required to achieve convergence

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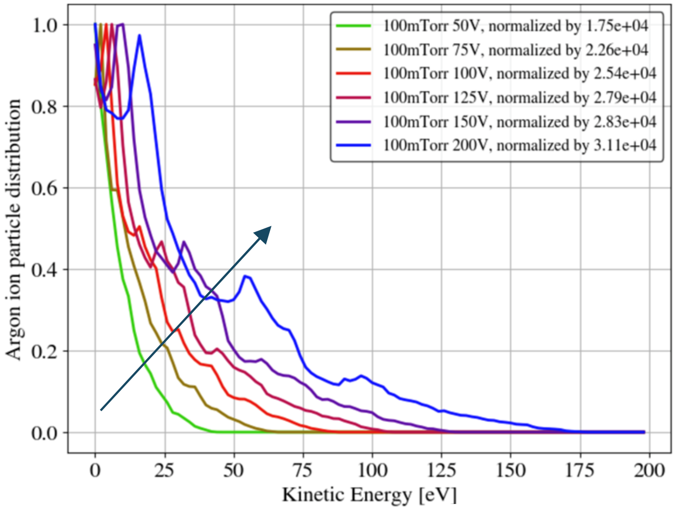
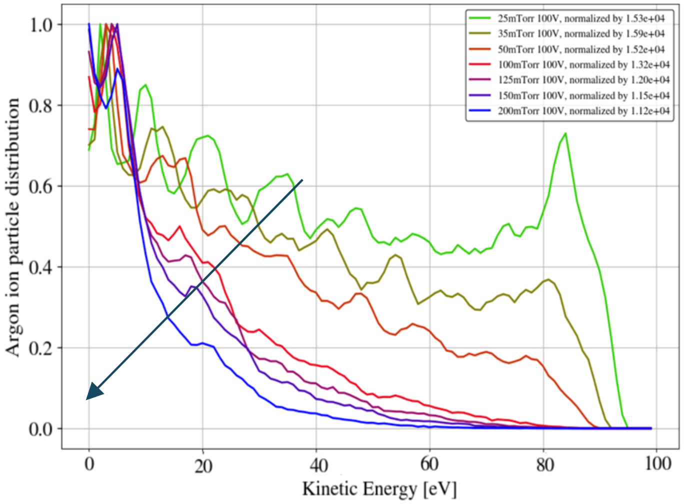
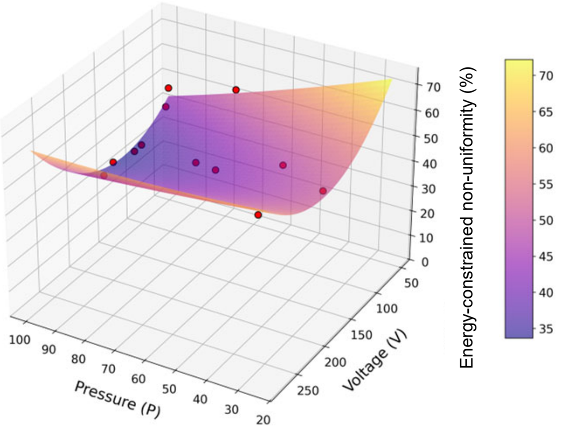
Energy-constrained uniformity optimization

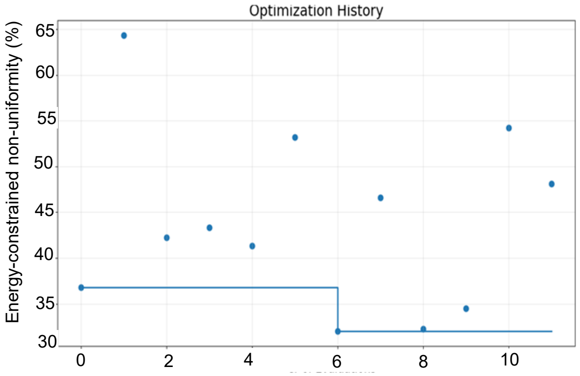
Effect of voltage on IEDF on powered electrode



Effect of pressure on IEDF on powered electrode

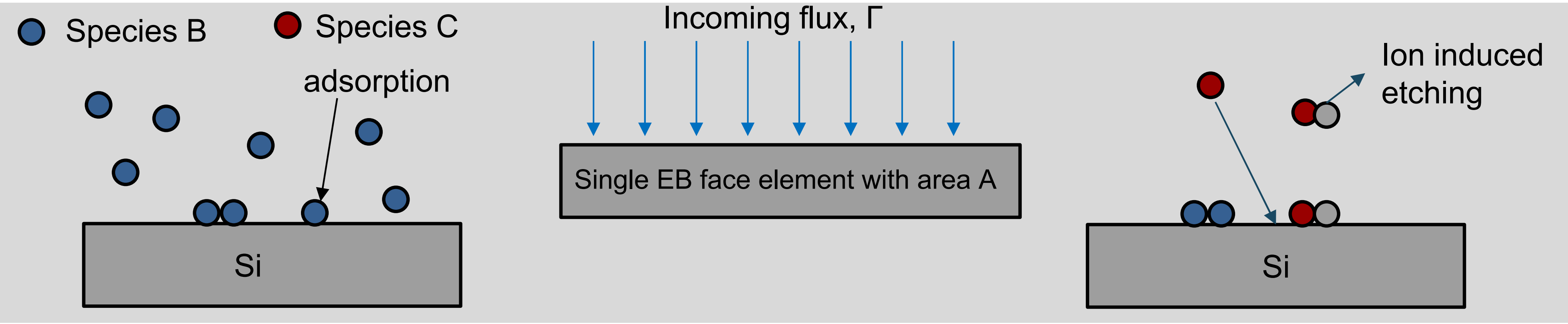






- Ion energies affect etch quality and precision.
- Low pressure, high voltage maximize uniformity – but ion energies are high
- Uniformity with energy constraints is important for fabrication

New surface physics module to capture etch evolution

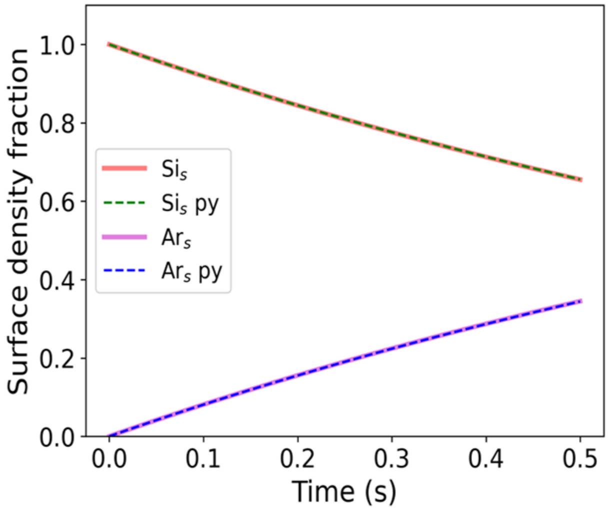


Reactions:
Adsorption and Desorption

$$Ar_g^+ + Si_s \rightarrow Ar_s$$

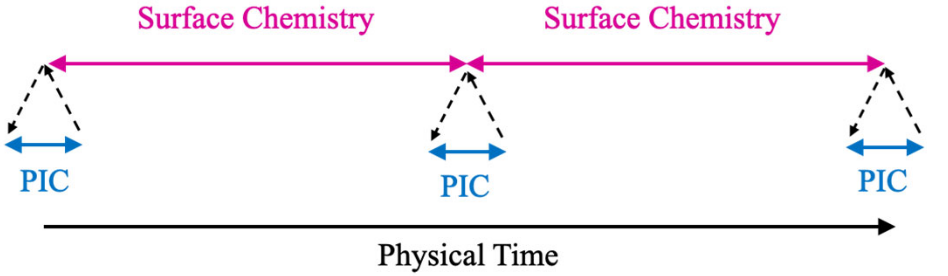
$$Ar_g^+ + Si_s \rightarrow Ar_g^+$$

Inputs:
Ar^+_g Influx = 10^{19} $m^{-2}s^{-1}$
Ar^+_g E_{in} = 40eV



Work-in-progress

Coupled PIC/MCC with surface chemistry using time-slicing



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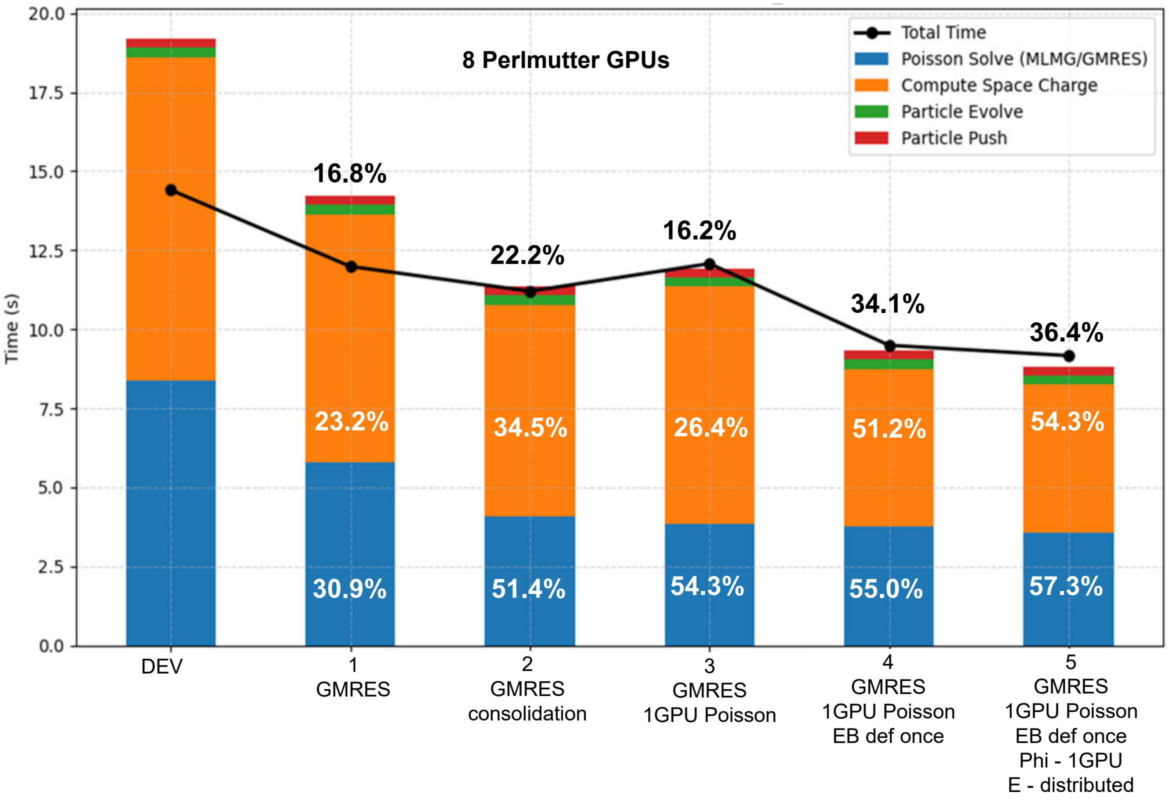
Algorithmic improvements for computational efficiency

Step-by-step improvements:

1. GMRES instead of MLMG for Poisson solve
2. Consolidation/agglomeration in GMRES cycle
3. GMRES + Poisson on 1 GPU (potential + E), communicate potential, Ex, Ey, Ez
4. Remove duplicate definition for EB for Poisson solve
5. Poisson on 1GPU, communicate potential, E on distributed GPU

Achieved ~37% speed-up > proposed speedup of 20%

Our solution : Poisson solve on reduced GPUs than particle methods – is broadly applicable for other electrostatic applications



Partnerships : National Lab, University, Industry

Dr. Ricardo Ruiz, Director,
CHiPPS, LBNL

Synergistic Activities:

Received Molecular Foundry User-Proposal award to perform plasma etch experiments using inductively coupled plasma reactor and compare with plasma-surface chemistry enabled PIC/MCC simulations

Dr. Sergey Averkin,
TEL Technology Center,
America, LLC

Awarded a **new HPC4EI project** in partnership with TEL Technology Center, for high-frequency plasma reactor studies.

Interest in work from researchers from **Applied Materials** and **LAM Research**, who may also benefit from the open-source, industry compatible BSD-3-Clause-LBNL licensing of our codes and workflows.

Alignment with DOE's Genesis Mission

Genesis Mission

National Science and Technology Challenge : Recentering Microelectronics in America

"An AI-driven full-stack co-design ecosystem will enable faster innovation cycles, de-risk ultra-efficient manufacturing processes and component design"

Our digital twin framework with ML-enhanced Bayesian optimization workflow with accurate kinetic modeling will enable process design and optimization
- accelerating lab-to-fab time
- reducing costly trial-and-error experiments (costly substrates, and energy-use)
- reducing discard-rate, increasing yield with high-precision etch
- boosting global competitiveness of chip manufacturing

It can fit into a larger workflow, where experimental measurements are also used to train models

Workforce development for microelectronics

- July 7 - July 11, 2025
- 21 high school students from the Berkeley Lab Director’s Apprenticeship Program / Interdisciplinary Pathways to Machine Learning and Data Science participated
- 10 LBNL researchers + 2 external researchers gave talks, led tours, or were part of the career panel

Faith Dukes
Task Lead

Alisa Betalle
Co-Lead

Corbin Shatto
Co-Lead

Revathi
Participant

Monday	Tuesday	Wednesday	Thursday	Friday
Introduction Relevance of microelectronics Evolution of microelectronics over the years	Modeling & Simulation of plasma reactor for etching - python scripting to visualize results Design and Materials Talk Device Materials Talk	Lithography Lab / Circuit Design Trainer Lab Center for X-Ray Optics Tour (Microelectronics patterning)	Lithography Lab / Circuit Design Trainer Lab Molecular Foundry Tour (Reactive ion etch devices for chip fabrication) Nanofabrication Facility Tour	Chips and System Modeling Talk National Energy Research Scientific Computing Center (NERSC) Tour Career Talk (public and viewed by other summer interns at Berkeley Lab) ~ 120 students

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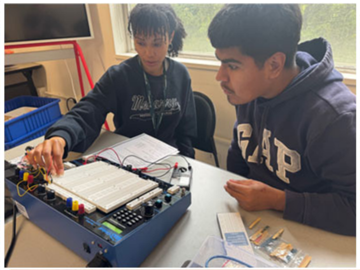
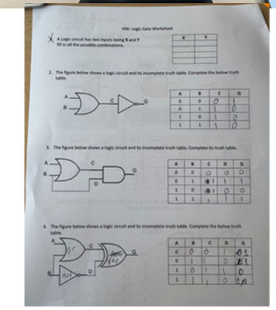
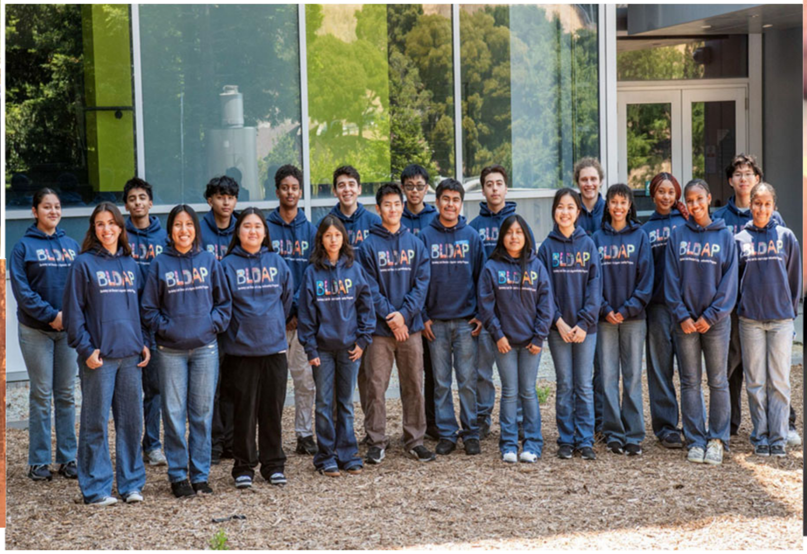
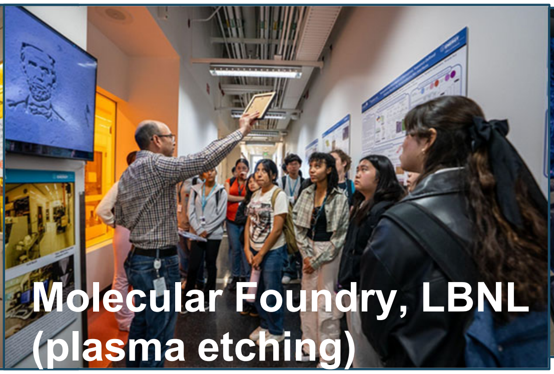






CXRO facility, LBNL
(photolithography)



Molecular Foundry, LBNL
(plasma etching)

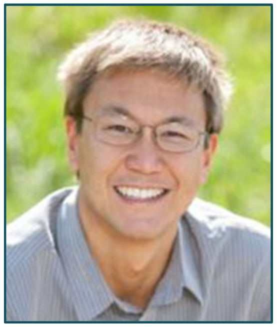
Perlmutter, NERSC, LBNL
Modeling & Simulation

Thanks to the team and funding acknowledgement

Revathi Jambunathan (PI)
Research Scientist,
LBNL

Richard Lombardini
Professor
St. Mary's Univ

Andy Nonaka
Staff Scientist,
LBNL



Remi Lehe,
Research Scientist,
LBNL

Andrew S. Fierro
Assistant Professor,
NMT Univ

Mark Kushner, (advisor)
William P Allis Distinguished
Professor, U. of Michigan

Andrea Diaz
St. Mary's University
SULI Intern at LBNL

Jorge Quiroga
Graduate student
NMT University

Tristan Jiron
Undergrad
NMT University

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FWP # 2025-LBNL-FP00019430

Thanks to the WarpX team & collaborators

Thank you !
Questions and comments
are welcome